Design and Performance Analysis of Memristor Based Non-Volatile SRAM Cell

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Abstract

Non-Volatile memories are gaining more importance in memory design due to their data retaining capability during power-down mode. Conventional 6 Transistor Static Random-Access Memory (SRAM) cell does not have Non-Volatile property. Memristor is one of the non-volatile techniques used in Non-Volatile SRAM (NVSRAM). This research deals with 7 Transistor and 1 Memristor (7T1M) based NVSRAM cell. Multi-threshold Complementary Metal Oxide Semiconductor (MTCMOS) power reduction technique was implemented to reduce the total power consumed in the circuit. Memristor was modelled using Verilog-A code in the Cadence Virtuoso tool and its hysteresis behaviour was obtained for the better Static Noise Margin (SNM) value. The designed Memristor was integrated with Volatile SRAM to realize NVSRAM cell. Both 7T2M and the proposed 7T1M architectures were analyzed for the delay, power, and SNM values. The proposed 7T1M NVSRAM cell has a higher SNM value of 0.518 V, whereas the 7T2M NVSRAM cell has the SNM value of 0.04V. Delay in the two architectures is nearly same. The 7T1M cell has slightly more power because the bistable element is directly connected to the ground. The 6T SRAM cell, 7T2M NVSRAM cell, 7T1M NVSRAM cell, and MTCMOS based 7T1M NVSRAM cell were implemented in Cadence Virtuoso tool at 45 nm technology with operating voltage 1.2V.

Keywords*: Memristor, NVSRAM (Non-Volatile Static Random-Access Memory), SNM (Static Noise Margin), MTCMOS, HRS (High Resistance State), LRS(Low Resistance State).*

1.0 Introduction

In VLSI design, memory plays a very important role. The critical issues associated with memories are operation speed, noise immunity, area, and power consumption. There are two types of memories SRAM and Dynamic RAM (DRAM). DRAM structure has a transistor and the capacitor. It has only one transistor and one capacitor. The capacitor is used for data storage by charging it. The main property of the DRAM is periodic refreshing. It is inevitable to refresh the DRAM after every cycle which increases the power dissipation of

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the circuit. So, the SRAMs are used for high-speed memory design to avoid periodic refreshing. The SRAM provides high read and write stability by using a bistable inverter element in its structure. These properties of SRAM make them preferable over DRAM [1]. A detailed study is reported on SRAM for selecting suitable architecture for the design. The study revealed that 6T architecture is preferred over the 4T architecture [2]. The 4T SRAM has less area but it has more power dissipation and higher write and read access time. Due to the more delay exhibited by the 4T SRAM cell, the 6T SRAM cell is used for the design which has a better noise margin, lesser delay, and also lower power dissipation. The volatile nature of the SRAM cell makes the cell to lose the data whenever the power goes off. So, to make volatile SRAM as Non-Volatile, different Non-Volatile techniques are to be used along with the conventional 6T SRAM cell. Then the cell will be able to restore the data after the power comes back. This feature of the cell is known as Non-Volatility.

Different Non-Volatile technologies to make the SRAM as NVSRAM are Ferroelectric RAM (FeRAM), Magnetic Tunnel Junction RAM (MTJ RAM), Memristor RAM (MRAM), Resistive RAM (RRAM) [3], Phase Change RAM, etc. A memristor is a Non-Volatile memory component that has the ability to restore the data back after power down. This Non-Volatility of the Memristor is got by changing its resistance during on and off mode thereby it stores the data when there is no power. The two resistance states of Memristor are the High Resistance State (HRS) and Low Resistance State (LRS). Memristors are widely used in many devices because it will add the Non-Volatile feature for that device that means the device can retain the memory without power. The Memristor will change its resistance state from HRS to LRS during its operation and it limits the current in one direction and increases the current in other direction. Memristors are considered as a sub-category of Resistive RAM(RRAM). Memristor has higher SNM and endurance than that of any other technologies. Thus, Memristor is widely used in Non-Volatile memory designs.

The NVSRAM is in demand because of its Non-Volatile property. Different Non-Volatile techniques are used to make SRAM as Non-Volatile. Amongst different models of Memristor, the VTEAM model showed better performance [4]. To overcome the volatile property of SRAM, the seven Transistor and two Memristor based NVSRAM has been proposed [5]. The 7T2M NVSRAM cell had a good read and write margins when compared to other NVSARM architectures but had a lesser value of SNM. To reduce the overall power of the NVSRAM circuit many power reduction techniques such as MTCMOS and Self Controllable Voltage (SVL) have been implemented [6] and the significant reduction in the total power is observed.

Passive elements like resistor, capacitor and inductor are the basic fundamental elements in circuit design. The Memristor acts like a fourth fundamental passive element [7].

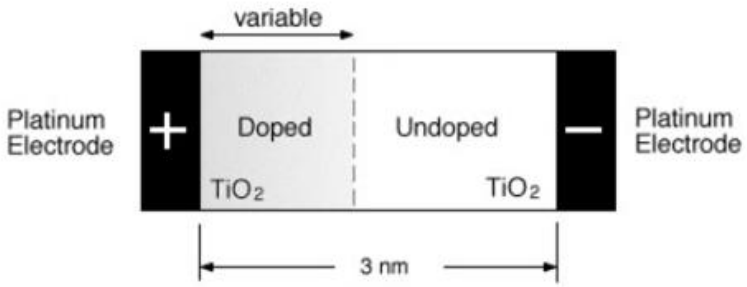

Fig. 1. Structure of a Physical Memristor [8]

The Memristor has two terminals: positive terminal and negative terminal. The positive and negative terminal of the Memristor is made of the Platinum electrode. The positive and negative terminal is decided based on the doping level of Titanium Dioxide (TiO2). The physical structure of a Memristor is shown in Fig. 1. If the TiO2 is heavily doped, then that side of the Memristor is the positive terminal and the opposite side is the negative terminal [9]. The doping concentration can be variable. When the high electric field is applied to the TiO2, its dopants try to move in the direction of the current. The applied voltage between two terminals makes oxygen atoms drift towards left or right and depending upon the voltage applied the material will become thicker or thinner. If the material is thicker, then the device is in the HRS state and if the material is thinner then the device is in the LRS state.

The SRAM is the basic component of the memory. The SRAM stores the data if the power is supplied to the circuit. This property of SRAM is known as volatility. There are many configurations of SRAM like 4T, 5T, 6T, and so on. Every configuration of SRAM has its advantages and drawbacks in terms of power, area, and delay. The 4T SRAM has a smaller on-chip area but the power consumption is very high. Therefore, 6T SRAM is concluded as the optimized design of the SRAM [10].

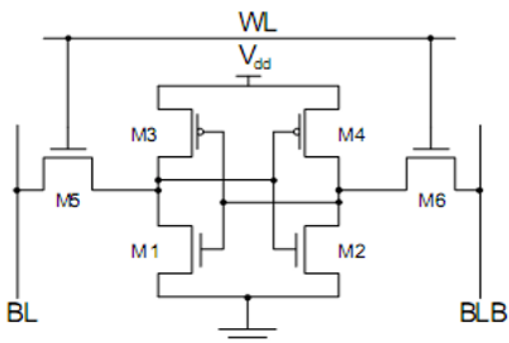

Fig. 2. Schematic of Conventional 6T SRAM circuit

The conventional 6T SRAM consists of two cross-coupled inverters [11]. As the inverters have two stable states that are '0' and '1', the 6T SRAM configuration is stable. It has both read and write phases of operation. In 6T SRAM cell, the inverter is connected to the bit line and the complementary line through the access transistors. Bit lines act as input during the write operation and as output during the read operation. The control of the access transistors is done with another line called word line which is used to control the read and write phases of the cell. Fig. 2 shows the schematic of a conventional 6T SRAM using the CMOS technology. The circuit operates at the voltage of 1.2 V.

6T SRAM can be analyzed in two modes of operations:

Write Mode: During write '1' operation, BL is made '1' and BLB is made '0'. After this word line is asserted to enable a write operation. The value on the bit line will be written to the device. This written value will be available at the output pin (Q and QB). During write '0', the above operation repeats with the initial value on BL as '0'. The BL will be pulled down to '0' by the pull-down transistors.

Read Mode: During the read operation, the bit lines are pre-charged to VDD/2. Later based on the stored value, the BL is either pulled down to the ground or pulled up to VDD by the NMOS or PMOS transistor respectively. The ratio of the pull-down transistor width to that of the access transistors width must be high for better read stability.

2.0 Proposed NVSRAM Design

Different models used to design Memristor are Linear Ion Drift Model, Non-Linear Ion Drift Model, Simmons Tunnel Barrier Model, Threshold Adaptive Memristor (TEAM) Model, and The Voltage Threshold Adaptive Memristor (VTEAM) Model. The VTEAM model has better results for Non-Volatile property because it has better SNM value in the Hysteresis curve. The equation used to design the VTEAM Model [12] is shown in mathematical expression (1).

$$i(t) = \left[R_{ON} + \frac{R_{OFF} - R_{ON}}{w_{off} - w_{on}}\left(w - w_{off}\right)\right]^{-1} . v(t) \qquad (1)$$

Which gives I-V relation of the Memristor. Here, R_{ON} and R_{OFF} are the resistance levels of the Memristor, and w_{off} and w_{on} define the boundary of state variable w.

The conventional 6T SRAM Cell is volatile because it doesn't have any storage element to store the data when the power goes down. To make the SRAM cell as Non-Volatile the resistive NVSRAM cell was introduced called as 7T1R cell. This cell has the Non-Volatile feature, but it suffers from the stability issues and it has higher power consumption due to the resistive component in it. To improve the stability of 7T1R NVSRAM cell, the Memristor based NVSRAM cell known as 7T2M NVSRAM has been designed. It has 7 transistors and 2 Memristors in its architecture. The architecture is shown in Fig. 3.

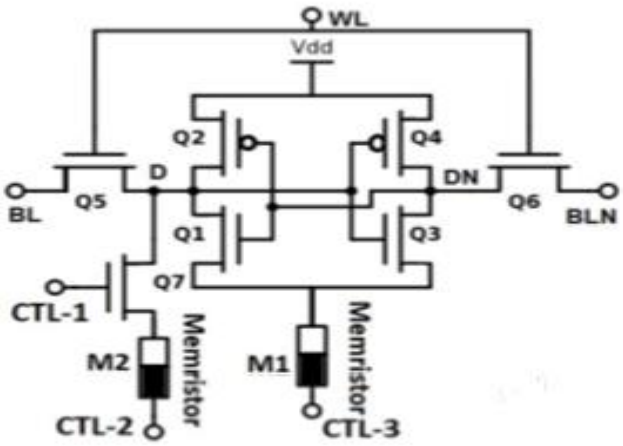

Fig. 3. Circuit structure of 7T2M- NVSRAM cell [5]

The architecture has one basic 6T SRAM cell, two Memristors (M1 and M2), and one pull-down NMOS transistor (Q7). The Memristor M1 positive terminal is connected to the source of transistor Q1 and Q3. The negative terminal of the Memristor is connected to the control input C3. In this architecture, there will be less power dissipation because bistable element is connected to Memristor M1instead of ground.

The Memristor M1 resistance states are changed using the control input pin C3. To keep M1 in HRS mode, the C3 value should be logic 1. To keep M1 in LRS mode, the C3 value should be logic 0. The output voltage swing of the NVSRAM cell depends on the HRS and LRS mode. The Memristor M2 is included in the design for the Non-Volatile operation of the 7T2M NVSRAM cell. The positive terminal of the Memristor M2 is connected to the source of pull-down transistor Q7 and the negative terminal is connected to the control input pin C2. The gate terminal of MOSFET is given to control input C1 and the drain of the transistor is connected to the output node of the SRAM cell. This Memristor is used as a Non-Volatile storage element for the SRAM since it stores the logic value of the output node of SRAM when the power goes down and when the power comes back it will restore to the output node value.

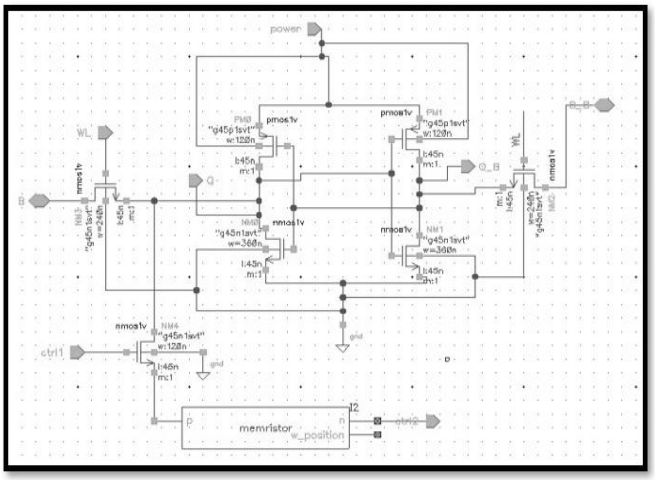

Fig. 4. Circuit structure of proposed 7T1M-NVSRAM cell

The proposed 7T1M-NVSRAM cell is shown in Fig. 4 and it operates in the following modes.

Write 1 mode: In this mode both the control input pins C1 and C2 are made off (logic 0) and the logic 1 value is written on to the memory cell by the bit line through access transistors. The Memristor logic storage action will not take place in this mode as control pin C1 has terminated the connection between the output line and the Memristor.

Store 1 mode: In this mode, the control input C1 is made logic 1 that turns on the transistor connected to the Memristor and the control input C2 is kept at logic 0. Now the Memristor has got the path to output node Q and the logic 1 value will be stored in the Memristor.

Power down mode: In this mode, the power supply (V_{DD}) in the circuit is made 0. Thus, the source of the PMOS transistor is connected to logic 0 and the output node Q goes down to logic 0. During this operation, the control inputs C1 and C2 are kept at 0 to make sure that Memristor is holding the previous output data value.

Restore 1 mode: In this mode, the power supply is made high i.e. logic 1. The control inputs C1 and C2 are made logic 1. The Memristor writes the previously stored logic 1 value onto the memory cell output node Q. Thus, the memory cell has been successfully got restored the value after the power-down operation.

Similarly, if the output node value is at logic 0 then we perform the same store, power down, and restore operations. But during restoring logic 0, the visual representation of output changing to 0 will not be there because of previous power-down operation. During power-down mode, the output node will be zero. So, restoring 0 after power-down mode does not have any impact on the output graph.

MTCMOS is the power reducing technique used in the CMOS designs to optimize the total power consumed in the circuit [13-16]. In this technique, two additional transistors called sleep transistors are introduced one at the top and the other at the bottom of the circuit. Both upper and lower transistors have complementary inputs. The upper transistor has a sleep input and the lower transistor has a sleep bar input. The transistors are made off during sleep or standby mode and the low Vt logic will be separated from the VDD and ground. Hence very less subthreshold current will be flowing in the circuit[17-18]. Thus, it reduces the total power consumption of the circuit. Fig. 5 shows the implementation of MTCMOS based 7T1M NVSRAM cell.

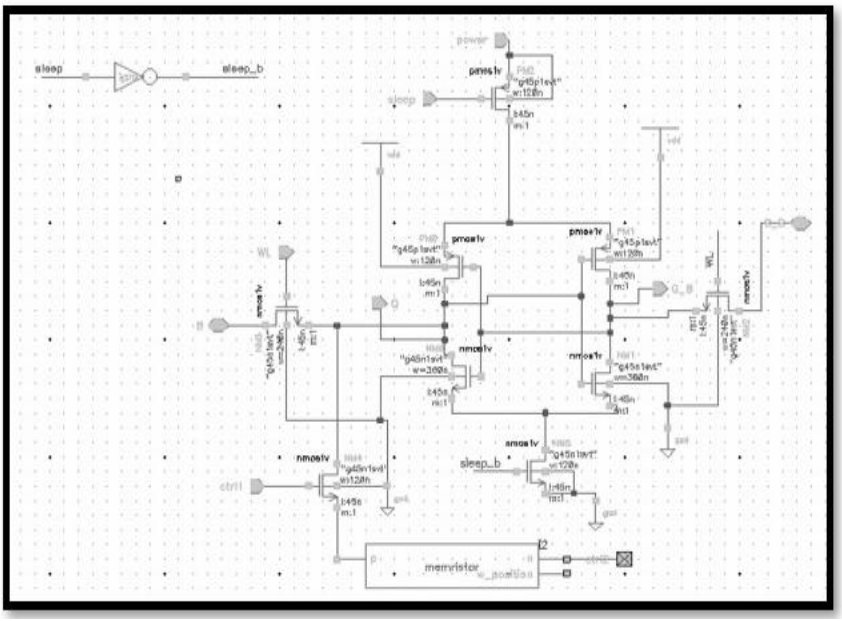

Fig. 5. Circuit structure of proposed 7T1M-NVSRAM cell with MTCMOS technique

3.0 Results and Discussion

The steps followed to get the Memristor hysteresis curve were:

1. Mathematical models such as Simmons Tunneling Model, Non-Linear Ion Drift Model, TEAM model, and VTEAM model were tried to get a better hysteresis loop for the Memristor. The VTEAM model provided a better hysteresis curve for the lower operating voltage of 1.2 V.
2. The Memristor model is designed in Cadence Virtuoso tool using Verilog-A code.
3. The symbol of the Memristor is created and obtained the hysteresis curve for operating voltage of 1.2V.
4. The obtained I-V curve of Memristor is shown in Fig. 6.

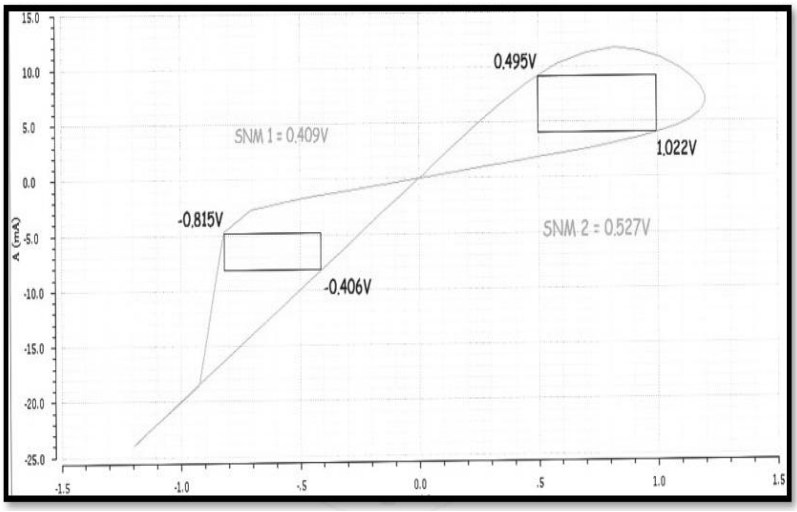

Fig. 6. Hysteresis curve of Memristor

The butterfly curve of the Memristor has two lobes with two different SNM's for each lobe. The SNM is the amount of noise voltage that the device can handle without distorting its output value. The minimum SNM of those two lobes is the SNM of the Memristor. Here SNM1 is 0.409V and SNM2 is 0.527V and hence SNM of the Memristor is 0. 409V. Table 1 depicts the parameters used for creating the Memristor model.

Table 1. Simulation Parameters of a Memristor

Parameters	Values
HRS(Roff) (kΩ)	62.5
LRS(Ron) (Ω)	50
Aoff	5
Aon	2
Voff (V)	0.02
Von (V)	-0.2
Woff (nm)	3
Won (nm)	0

Fig. 7 shows the operation of the 6T SRAM cell. When pre-charge is 0, the bit and bit bar line get charged to VDD/2. When the write/read bar is 0, SRAM is in the read mode and the bit line reads the content of the output line when the

word line is asserted. When the write/read bar is made high the SRAM is in write mode. It writes data onto the memory when the word line is asserted.

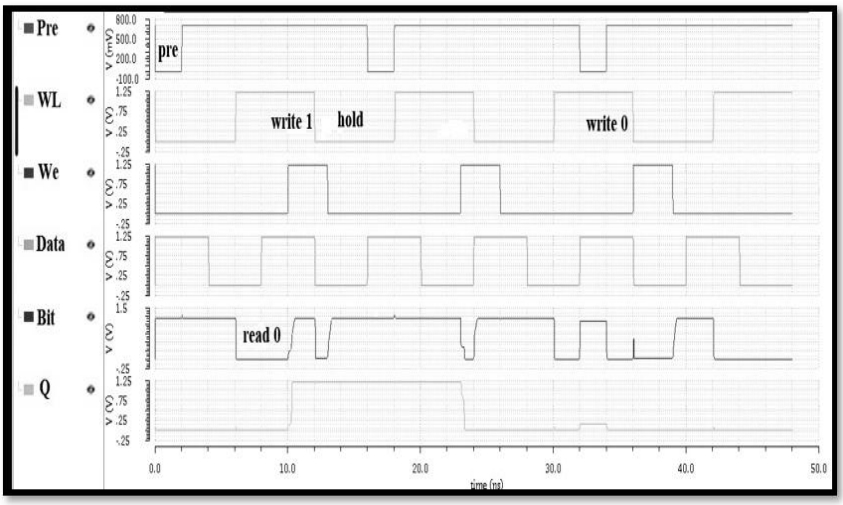

Fig. 7. Read and write operations of a 6T SRAM

Fig. 8 shows the hysteresis curve of the 6T SRAM cell. SNM of the cell can be calculated by Min (SNM1, SNM2). Hence, SNM of the 6T SRAM cell is 0.502V. Fig. 9 shows the hysteresis curve of a 7T2M Non-Volatile SRAM cell. The SNM of 7T2M architecture is 40mV. This architecture will improve the stability of the cell but the SNM of the cell is very less. The proposed 7T1MNVSRAM architecture will improve the SNM of the cell.

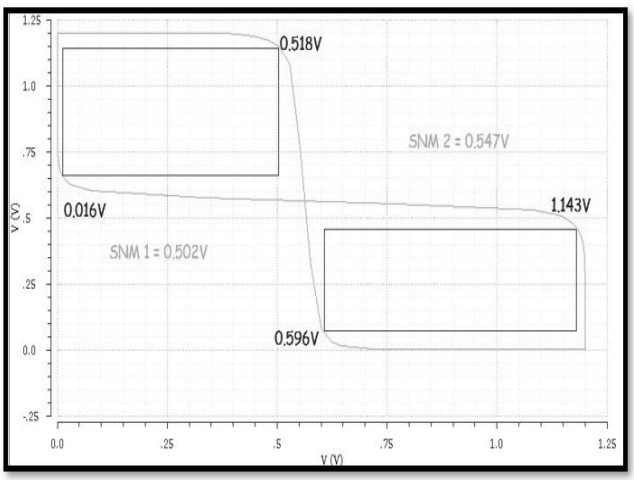

Fig. 8. Hysteresis curve of 6T SRAM

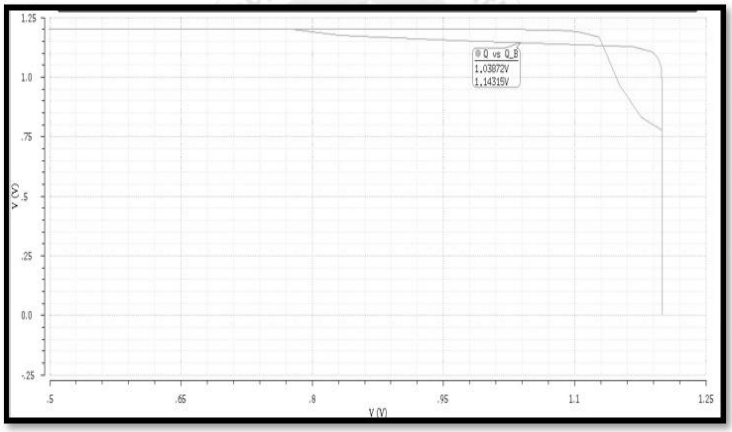

Fig. 9. Hysteresis curve of a 7T2M-NVSRAM cell

7T1M NVSRAM cell Read and Write operations can be analyzed in four modes namely Write, Store, Power down, and Restore modes. During Write 1 mode, the SRAM will store the logic 1 value and the memristive action will not take place in this mode. During Store 1 mode, the Memristor stores the logic 1 value. During Power down mode, the power supply is made zero so that the output of SRAM cell goes to logic 0. During Restore 1 mode, the Memristor will help to restore the output node value to logic 1. The Fig. 10 shows the output operation of the 7T1M NVSRAM cell. Fig. 11 shows the hysteresis curve of the 7T1M-NVSRAM cell. The SNM of the 7T1M-NVSRAM cell is 0.518V.

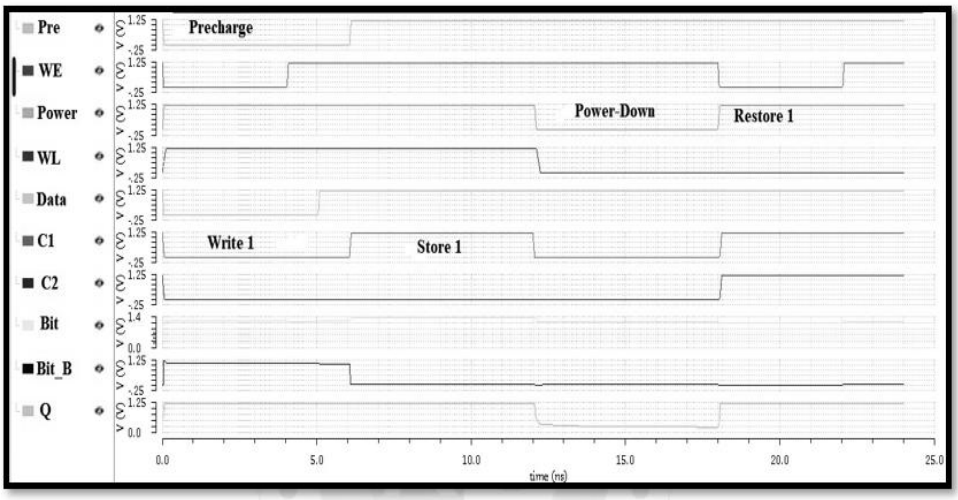

Fig. 10. Read and write operations of a proposed 7T1M-NVSRAM cell

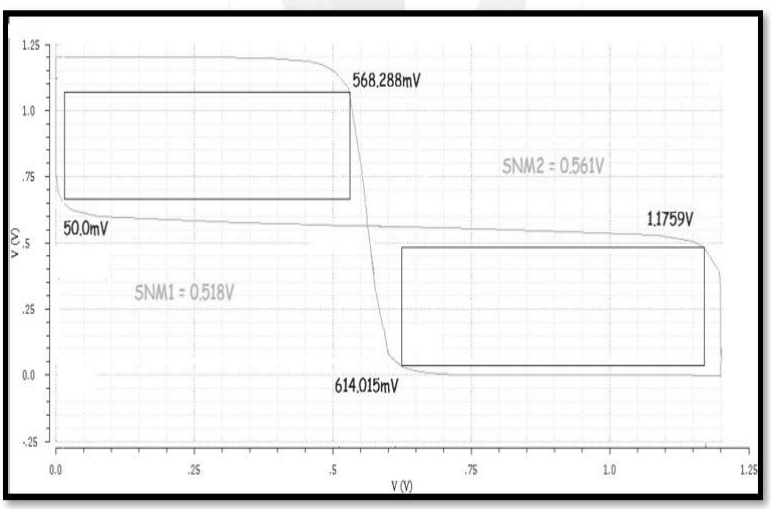

Fig. 11. Hysteresis curve of proposed 7T1M-NVSRAM cell

The proposed 7T1M-NVSRAM cell, 7T2M-NVSRAM cell, and 6T SRAM structures were simulated in the Cadence Virtuoso tool at 45nm technology, and various performance parameters such as Read Access Time (RAT), Write Access Time (WAT), power and SNM are measured. The RAT of the proposed 7T1M-NVSRAM is optimized so that it requires lesser time to perform the read operation compared to 7T2M-NVSRAM cell and also WAT required for both the architecture are almost similar. The obtained values of SNM for 6T SRAM, 7T2M-NVSRAM, and proposed 7T1M-NVSRAM are 0.502V, 0.04V, and 0.518V respectively. This shows that the Proposed 7T1M-NSRAM has a higher SNM value compared to 7T2M-NVSRAM and 6T SRAM. The power value of 7T1M is slightly higher because the NMOS transistors of the 6T SRAM cell are directly connected to the ground. The power can be optimized by using power optimization techniques like MTCMOS and SVL techniques. The comparison of the performance parameters of a different architecture is listed in Table 2.

Table 2. Comparison of Results

Design Specifications		6T SRAM Cell	7T2M NVSRAM	Proposed7T1M NVSRAM
Read Access Time	Restore 0	0.054nS	0.154nS	0.150nS
	Restore 1	0.037nS	0.50nS	0.124nS
Write Access Time	Write 0	0.260nS	0.145nS	0.167nS
	Write 1	0.272nS	0.145nS	0.161nS
Power		9.33uW	23.05uW	38.31uW

PDP (Power DeLay Product)	2.48 fsW	5.439 fsW	5.765 fsW
SNM	0.502V	0.04V	0.518V
Area (Number of circuit elements used)	6 Transistors	7 Transistors, 2 Memristor	7 Transistors, 1 Memristor

4.0 Conclusion

In this paper, the 7T1M NVSRAM cell is proposed by integrating one Memristor and one pull-down transistor for the conventional 6T SRAM. The VTEAM Model-based Memristor has been designed and obtained a higher SNM value of 0.409V. The proposed NVSRAM cell has been compared with 7T2M NVSRAM cell for Power, Delay, SNM, and Area. The Read and Write Access time of both the architectures are almost same with the compromise of power. The power reduction technique MTCMOS is employed to the proposed NVSRAM cell to reduce the power consumption of the cell. The proposed 7T1M NVSRAM cell has the SNM of 0.518V, whereas the 7T2M NVSRAM cell has the SNM of 0.04V. The 7T2M architecture uses two Memristors whereas the proposed 7T1M NVSRAM cell has only one Memristor. Therefore, the proposed NVSRAM cell has a better SNM value and lesser area when compared to the existing 7T2M NVSRAM cell.

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