High Linearity Class-E Power Amplifier using Linear-mode Predistorter at 1.9 GHz

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Abstract

This research proposes a highly linearized Class-E Power amplifier operating at 1.9 GHz using 0.5 µm Enhancement-mode GaAs pHEMT technology with simplified matching elements, reduced die size and complexity. Wider bandwidth is achieved through reactance compensation load network of Class-E PA. A basic Class-E power amplifier is built at 1.9 GHz and simulated using Advanced Design systems. Class-E configuration gives an output 1dB compression point of 20 dBm and input power @1dB of -6dBm respectively. Nonlinearity is taken care of introducing a linear-mode pHEMT based linearizer in the input bias circuit of the power amplifier which controls the gain deviation for different control voltages given at gate terminal of pHEMT. The amplifier integrated with linear mode pHEMT linearizer results in third order intermodulation distortion (IMD3) suppression around 49dBc, which is 25dBc higher than that of basic Class-E amplifier. Layout simulation of linearized Power amplifier is performed and results are verified with the schematic results. Highly linearized switching power amplifier of smaller size is realized with dimensions 1.69 x 2.65 mm^2 compared to that of any other conventionally (system level linearization) linearized Power amplifiers.

Keywords: *Input Intercept point, Linearizer, Output at 1dB compression point, pHEMT*

1.0 Introduction

Power amplifier is most power-consuming device in any wireless transmitter, which affects the battery power of the mobile devices. Higher efficiency achieved near saturation region leads to intermodulation components. Frequency-dependent distortions are produced due to nonlinear memory effect. Inherent nonlinearity found in diode junctions in the active devices produces harmonics and distortion

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when the applied input power increases [1, 2]. Nonlinearity is due to major three nonlinear elements of the MOSFET devices-transconductance gm, Device drain capacitance Cd and gate capacitance Cgs [3].

A few system level linearization techniques such as Back off, Feedforward, Predistortion, LINC have been developed to achieve linearity in PA. Among these, Predistortion technique has lower complexity and high power efficiency. The Predistorter linearizer provides inverse characteristics of amplifier so that it compensates for the amplifier's Non-linear characteristics. Reactance compensation technique is introduced in class-E amplifier which achieves wide bandwidth and high efficiency using LDMOS transistor technology operating at 136-174 MHz FM radio applications [1].

Cold-mode HEMT linearizer enhances 1dB compression point of the power amplifier (PA) with insertion loss (IL< 2 dB), with smaller size and minimum power consumption, is proposed [2]. Different types of diode-based and FET Predistorters are compared in terms of output power and linearity [3]. Amplifier design involves MESFET, varactors, and voltage variable resistors [4]. Higher bandwidth of 2.5 GHz and carrier to Intermodulation ratio greater than 10dB in TWTA and minimal phase change of fewer than 5 degrees has arrived. The design with linearizer involves an RF short provided by a capacitor and base-emitter diode of transistor, improves linearity with adjacent channel power ratio of 46 dBc at the output power of 28 dBm in both PCS and WCDMA bands with lower power consumption [5].

Intermodulation distortion cancellation is achieved by a Schottky diode in ROF systems [6]. The IMD3 suppression and dynamic range are enhanced by -26 dBc and 7.5 dB at 2.4 GHz respectively. For layout design, layer specifications for 0.5µm GaAspHEMT are referred from [7]. Harmonic termination circuits are used to improve the efficiency in class E design [8]. Alternate designs on load networks for wide bandwidth are studied from papers [9, 10]. Different predistortion methods using Schottky and PIN diode based RF Pre-distortion linearizer for TWTA is discussed [11].

Analog Pre-distortion techniques are studied in which Diode based linearization techniques for Power amplifiers are implemented with different technologies. With respect to circuit level linearization, IMD3 suppression ratio of 48dBc is achieved with Power amplifier using Harmonic injection technique [8]. In this research, circuit level linearization technique is designed and implemented to achieve higher

IMD3 suppression with less complexity and small die size. A low complexity linearization technique integrated in the power amplifier proposed results in smaller size and wide bandwidth operation compared with any other conventional methods.

2.0 CLASS-E Power Amplifier Design

Transistors act as switches which have potential for providing improved efficiency but they are not ideal switches. To prevent dissipation losses, the switches must be fast with respect to the frequency of operation. Class-E amplifier is basically used as switches which results with low power consumption since output current and voltage are exactly out of phase. To decrease the power dissipation, the circuit can be modified to force a zero switch voltage for a nonzero interval of time about the instant of switching. The specifications of Power amplifier at 1.9 GHz are presented in Table 1.

Table 1. Specifications of Class-E power amplifier

Parameter	Typical value
Higher Linear Gain	15 dB-30dB
Power at 1dB compression point	16 dBm-26 dBm
Maximum transmitted power (for power class 2 of PCS band) Ref. [3GPP TS 45.005 version 9.12.0 Release 9].	24dBm ($\pm$ 3dBm)
Application	Power class -2 PCS band 1900-1910MHz
PAE	15%- 80%
3rd order Intermodulation suppression (IMD3) (Δf= 20 KHz)	30dBc-50dBc
Linearity OIP3	24 dBm-40 dBm
Input Return loss S(1,1)	<10 dB
Output Return loss S(2,2)	< 10 dB

2.1 Load Network Design

A simplified equivalent load network, one with shunt resonant circuit L_1 and C_1 is followed by a series resonant circuit L_oC_o and load resistance R_L as shown in Fig.1. The reactances of shunt and series resonant circuits are varied with frequency and tuned to the fundamental frequency. The reactances are increasing and decreasing for series and shunt resonant circuit near the resonant frequency ωo. By proper selection of shunt circuit components, change in reactance with respect to frequency is controlled and exactly inverse to the response of the series circuit, there

by variation over a wide range of frequency is zero. This leads to wide bandwidth operation.

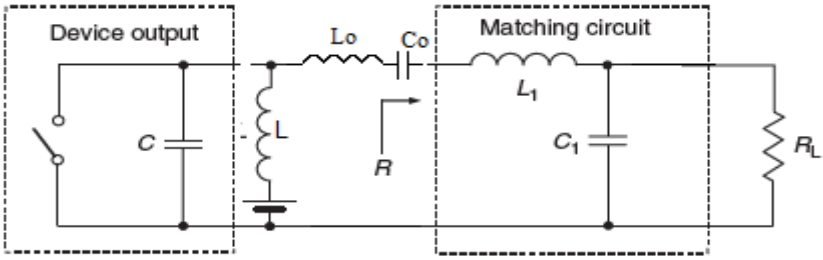


Fig. 1. Equivalent circuit of Reactance compensation network [1]

The values of reactance compensation network using formulae [4] are presented in Table 2.

Table 2. Computed values of load network components

Load network components	Value
Shunt capacitance C	0.998 pF
Series inductance Lo	2.2nH
Series capacitor Co	0.91 pF
Matching capacitor C1	2.04 pF
Matching Inductor L1	8.4 nH

The parallel circuit configurations directly match with the broadband conditions of Class E. As the load network of the parallel circuit configuration is similar to reactance compensation network, the design equations can be obtained [1].

2.1.2 Transistor Linearizer

When the input power applied to amplifier increases, the output gain and phase of amplifier decreases and increases respectively leading to nonlinearities. The Nonlinearity is compensated by the predistorter connected in series with the power amplifier. An MMIC pre-distortion linearizer using a pHEMT structure comprises of linear mode pHEMT (M2) with bias resistors R1 and R2. The gate bias for the M2 transistor (first stage of power amplifier) is applied through pHEMT linearizer. The M2 transistor serves the amplification stage of PA. The transistor linearizer comprises pHEMT (M1) with two bias resistors R1 and R2.

The two bypass capacitors C1 and C2 are present along with bias voltages control voltage Vc and gate to source voltage Vgs respectively. The M2 transistor serves the amplification stage of PA. Fig.2 shows a transistor linearizer circuit with its equivalent circuit model, connected to the gate stage of the M2 transistor of Power amplifier.

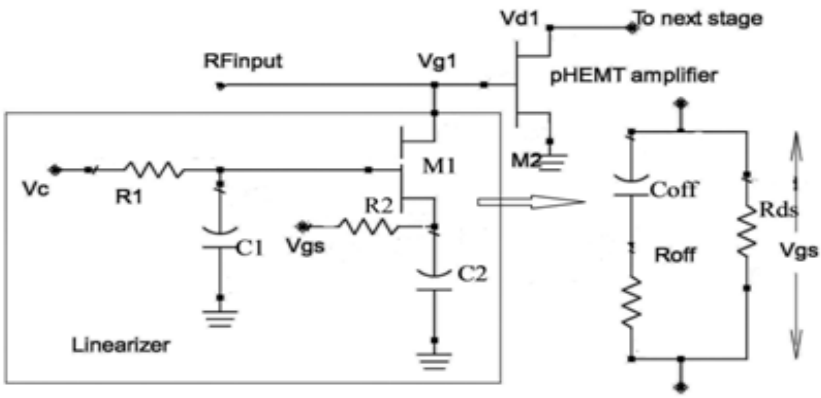


Fig. 2. Linearizer circuit using pHEMT

The equivalent circuit of pHEMT comprises Roff, Coff and current source [2]. The current source can be replaced by RDS whose value is 300Ω for eight fingers 150 µm pHEMT WIN semiconductors handbook [7]. The drain to source resistance RDS is obtained from the DC transfer characteristic curve as given by equation (1)

$$R_{DS} = \frac{1}{\partial I_{ds} / \partial V_{ds}} \tag{1}$$

As signal power increases, slope of dc transfer curve increases, which increases RDS. The gain expansion happens due to increase in RDS. The variation of Coff and Roff is less compared to RDS of the HEMT when input power is increased; therefore Coff and Roff are assumed to be constant in this study. The forward gain S (2, 1) for linearizer equivalent circuit in Fig.2 is obtained as shown in equation (2):

$$S_{21} = 2/2 + Z_0 \left(\frac{1}{R_{DS}} + \frac{1}{\left((1/j\omega C_{off}) + R_{off} \right)} \right) \tag{2}$$

where Zo is 50-Ω characteristic impedance. From the equation (2) it is clear that gain expansion of linearizer is achieved with increased RDS value. The power amplifier gain compression can be controlled by

employing a Linearizer in the input stage. The gain expands when the input power increases as shown in Fig. 3. The impedance at the drain terminal of pHEMT Linearizer is measured from S-parameter analysis.

Output impedance from smith chart is Zo*(0.121-j0.017) equal to 57.75-j33.4ohms.The Gate impedance of first stage pHEMT of Power amplifier is Zo*(0.296-j0.075) which is 14.8-j3.75. The impedance matching between the pHEMT Linearizer and first stage of power amplifier is done through a matching network comprising of spiral inductor and capacitor. The Insertion loss is reduced due to matching and improves the gain of the circuit.

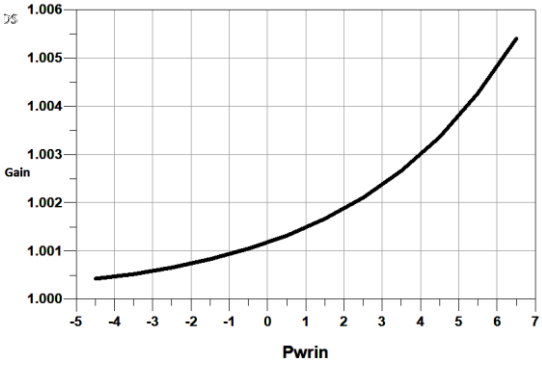
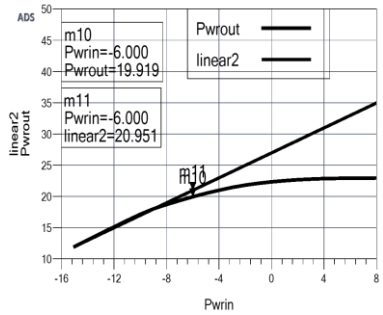
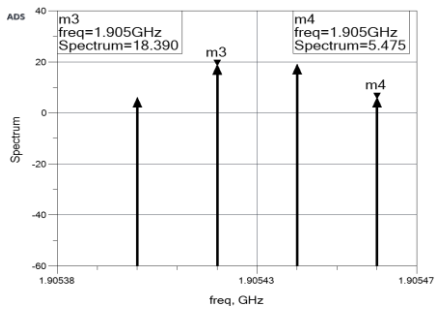


Fig. 3. Gain expansion with respect to Input power

3.0 Simulation of Class-E Power amplifier

The class-E power amplifier using WIN PDK PD5001 Enhancement CPW Transistor is simulated. Matching circuit is designed using smith chart utility and Reactance compensation method is used to design the load network. The component values are calculated using design equations [1] and optimization The class-E two-stage power amplifier is designed using 0.5µm pHEMT that results in the maximum output power of 20dBm and small signal gain S (2, 1) of 21dB.





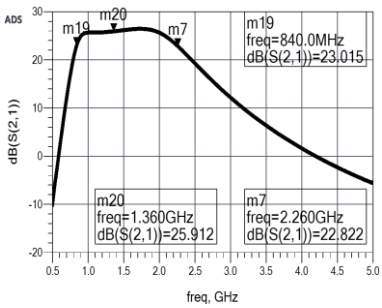


Fig. 4. a) 1dB compression point of Class-E PA, **b)** Two-tone spectrum and **c)** Gain S (2,1) vs. Frequency

The input and output return losses (S1,1 and S2,2) of -10 dB and -12 dB at 1.9 GHz obtained respectively. The Fig.4a shows the 1dB compression point has arrived at -6dBm input power (IP@1dB) with an output power (OP@1dB) of 20dBm.Two-tone analysis performed for the frequencies f_1=1905.42MHz and f_2=1.905.44MHz. The frequency offset of 20 KHz is chosen for Two-tone simulation. The Fig.4.b shows the third order intermodulation distortion suppression obtained as 23.7dBc.The Fig.4.C shows the gain S (2,1) plot which exhibits a wider bandwidth of 1.42GHz.

3.1. Simulation of Linearized Power Amplifier

The Schematic diagram in Fig. 5 shows the Class-E Power amplifier with pHEMT linearizer circuit. The output power reaches saturation at a higher input power of 9dBm, which is-6dBm in case of PA without linearizer. The Gate bias for the amplifier stage is given through a pHEMT transistor circuit whose control voltage varies the gain deviation of the circuit. The Vc of pHEMT (M1) set to be 1.2V, Input biasing voltage (vgs) as 0.9V for M1.The gate to source (VGS1 &VGS2) and drain bias voltages of pHEMT PA of 0.6V and 5V respectively.

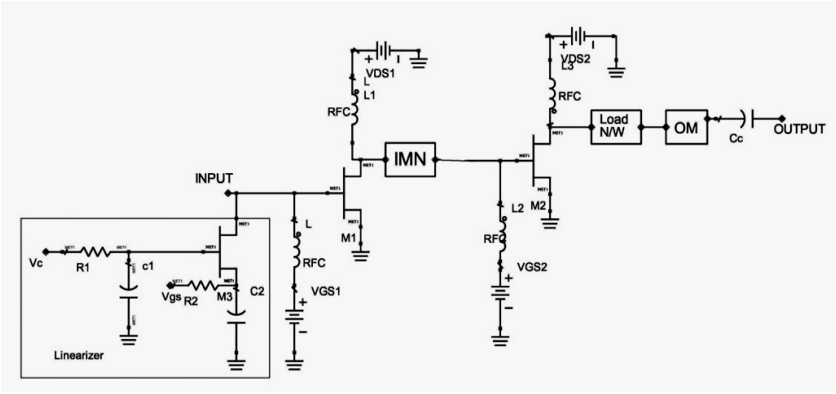


Fig. 5. Class E Power amplifier with pHEMT linearizer circuit

The inductive degeneration in PA exhibits a good input return loss and less noise figure. The IMD3 cancellation with linearizer is obtained as 49dBc which is 25dBc higher than for Class-E power amplifier. The output power (OP@1dB) of 22 dBm and input power (IP@1dB) of 9dBm has resulted with power gain of 15 dB at 1.9 GHz. Fig.6 a,b shows 1dB compression point and Two tone spectrum.

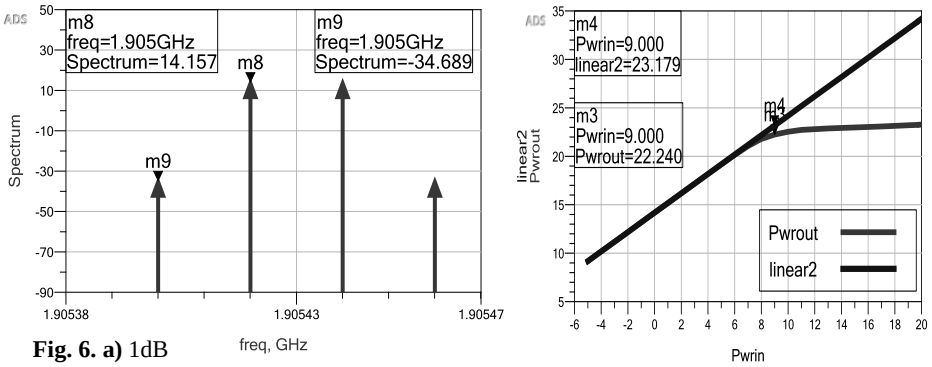


Fig. 6. a) 1dB compression point of Class-E PA with built-in Linearizer and **b)** Two-tone spectrum

4.0 Layout Results

The layout is constructed using PD-01 0.5µm GaAs Enhancement mode pHEMT Technology developed by WIN semiconductors Corporation, Taiwan. The layout involves models of spiral Inductors, Square Inductors, MIM and stack Capacitors, MLIN, MCORN, MTEE Junctions, BackVia, ViaM1-M2 are used by taking their values with reference to Class-E amplifier with microstrip lines. The layout is shown in Fig.7.

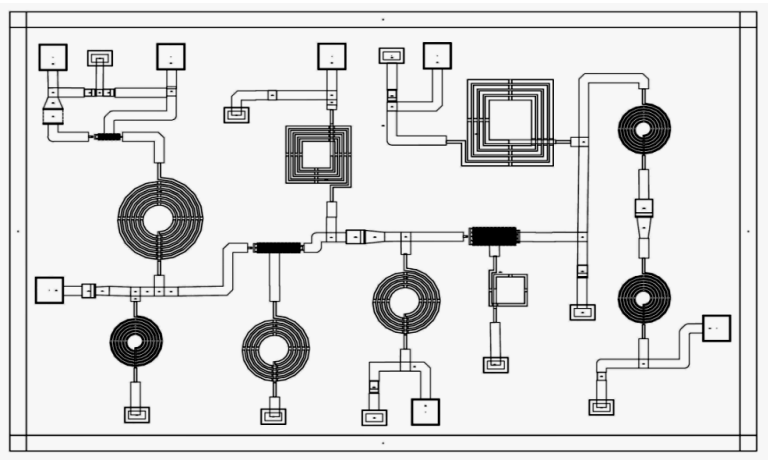


Fig. 7. Layout of Class -E Power amplifier with linear-mode pHEMT linearizer circuit.

The EM simulation of Class-E power amplifier is performed by the following procedure as shown below,

- Choice of PD-500X substrate
- Setting the EM setup as Momentum RF
- Set up of frequency plan to be 1GHz-6GHz, since the center frequency of the design is 1.9GHz.
- The cells/wavelength is chosen to be minimum 10.
- EM model is created for the layout without active elements. The Input and biasing ports are placed at the appropriate places.
- In the schematic window, the symbol of design is placed. The Active devices along with input and output ports, biasing voltages are applied.
- Circuit simulation is performed by including simulation controllers and results are verified.

Co-simulation is performed at 1.9 GHz. The layout designed for power amplifier with pHEMT based pre distorter has arrived to the dimensions of 1.69 x 2.65 mm^2. Co-simulation results of pHEMT linearized class-E power amplifier provides an IMD3 suppression is 36.5dBc, The output power and IMD3 suppression is reduced as shown in Fig.8 which is due the transmission lines used with characteristic impedance of 75 ohm.

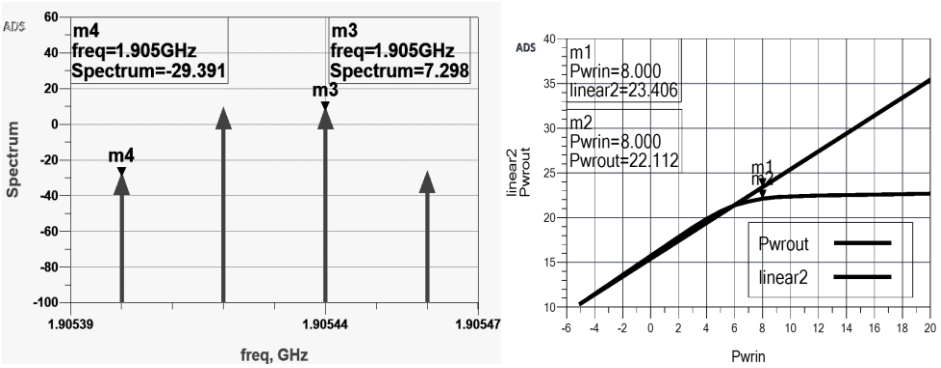


Fig. 8. a) Two-tone spectrum of Class E PA with built-in Linearizer and **b)** Return losses

5.0 Conclusion

Class- E power amplifier combined with built-in predistorter showed better linearity with the IMD3 cancellation of 49dBc at the center frequency of 1.9 GHz. There is an improvement of output power around 3dBm with respect to PA without linearizer at 1dB compression point. Layout co-simulation was performed and IMD3 suppression was found to be less than that of the simulated results. The gain is reduced as linearity and output power has the trade-off. The designed Class-E power

amplifier achieves a higher gain of more than 22dB over a bandwidth of 1.4GHz which encapsulates more than a single band (PCS/CDMA and band 2, 33, 35, 39 of LTE). Layout optimization can be carried out to compensate the gain reduction in the circuit and choice of standard microstrip line impedance also improves the better power output. The IMD3 suppression can be achieved better in layout results by choosing proper impedance values for the microstrip lines. Complexity and size of proposed PA are less than any other system level linearization techniques such as Feedforward, and Feedback.

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