Test Development for Power Management Integrated Circuit

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Abstract

Integrated circuits (IC) are the building blocks of electronic devices such as workstations, mobile phones, personal computers, automation hardware, automotive subsystems, military hardware, and home appliances. Each IC must meet the technical specifications during manufacturing. Even a single defect in IC can cause system failure. Hence, testing environment has to be developed. The aim of this research was to create a testing environment for testing the Smart High Side Switch which is a Power Management IC. A test program was developed to verify all the specifications as mentioned in the database. The device was characterized for quality and life span. The testing was done on Eagle Test Systems Automatic Test Equipment.

Keywords: *Power Management IC, Automatic Test Equipment (ATE), Eagle Test Systems.*

1.0 Introduction

Testing is an integral part of the IC manufacturing process [1]. Test coverage is an important metric in testing of IC. It is a list of potential flaws that do not take the features of the test plan. This list is crucial as it establishes a standardized system for calculating coverage measures and making comparisons. Coverage is determined by analyzing the capacities of each test case, not covered during the fault list creation. For the implementation of test solutions for ICs, several electronic testing concepts such as built-in self-test (BIST) [2], Mixed-signal ICs play an important role in the electronic industry [3], design for testing (DFT) [4 - 5]. To successfully cover all flaws in an IC, the testing method necessitates skill in the areas of RF signal testing, high current testing, and fast transient testing [6].

Testing of IC can be classified into three types, namely, production testing, bench testing and characterization. Production testing is the process of

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testing the fundamental parameters of each IC in which test time is an important aspect [7], and hence only basic parameters are tested in this stage. This testing is usually mechanised and performed at room temperature. Production Testing can be automated by using handlers to place IC on the analyzer and Automatic Test Equipment (ATE).

Bench testing is carried out to identify flaws in the structure and to approve the design plan on silicon. All the detailed features of IC are tested in bench testing. It is carried out in large-scale IC assembly. Characterization is performed to test the performance of IC at different temperatures and the model parameters are examined in the working range of temperatures. It can be accomplished in manual test setup or on ATE for which Automatic test pattern generation (ATPG) is essential [8-9]. Building test hardware entails creating a hardware interface board (HIB) [10-11] that allows the tester to interact with the Device Under Test (DUT). Multi-site testing employs parallel testing concept to minimize test time and cost.

ATE is used to automate testing of an IC (DUT) [12]. A Personal Computer (PC) or a master controller that synchronizes the source and the measuring equipment is used in an ATE. An automated machine known as a prober or handler connects the DUT to the ATE, aswell as an Interface Test Adapter that connects the ATE's assets to the DUT [13]. There is a sea change in ATE with different architectural adjustments to improve its capabilities. ATE must be developed in the same frequency range to cover all test cases and hence provide improved coverage. One of the most significant characteristicsof an ATE is that it must imitate test circumstances in severe temperatures which necessitates thermal cycling in order to test across temperature. For better results, ATE has to be accurate, and the signals generated should not have any jitter components.

High Side Switch is a power switch which provides an electrical connection from a voltage source or ground to a load. Smart High Side Switch is one of the topologies of Power Switch. The device is a fully protected high side power switch, with integrated NMOS power FET targeted for the intelligent control of loads. Accurate current-sense and programmable current limit are the differentiating features. Internally designed high-accuracy current-sense function enables for greater real-time monitoring effect. The functional block diagram of High Side Switch is shown in Fig.1.

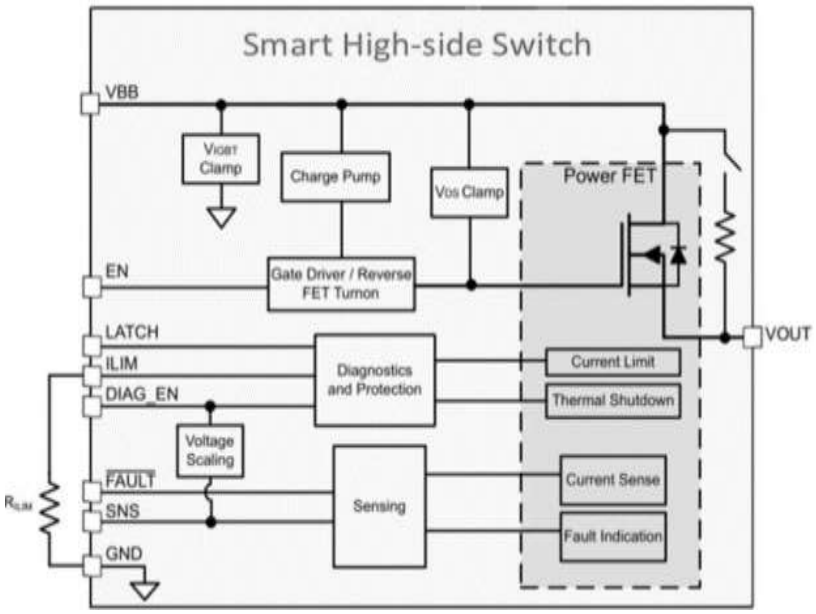

Fig. 1. Block diagram of High Side Switch

Protection features of High Side Switch include overload and short-circuit protection, Under Voltage Lockout (UVLO) protection

- Thermal Shutdown and Swing with self-recovery
- Loss of GND, Loss of supply protection
- Reverse Battery Protection with external components

2.0 Test Methodology

The automatic test program has been developed based on the Test Plan and the platform selected. The accuracy of the tester is improved by upgrading several test procedures, and the FT (Final Test) software is generated. Flowchart strategy for Final Testing is appeared in Fig. 2.

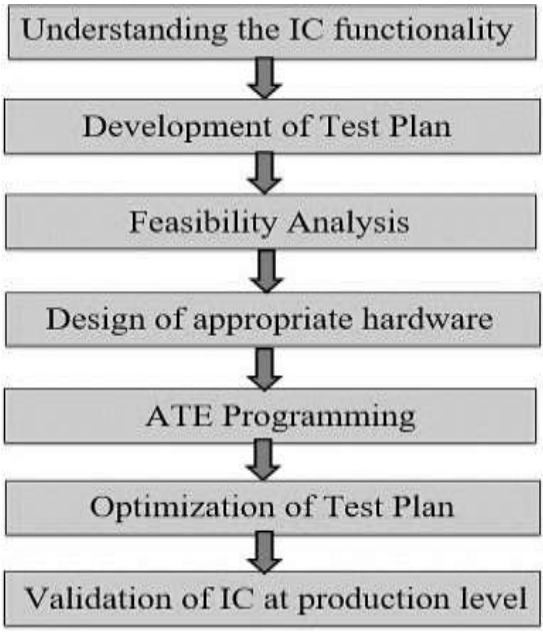

Fig. 2. I C Testing Methodology Flowchart

3.0 Implementation of Tests

Manufacturing Defects Test

Continuity Test: Before any quality analysis tests, continuity test must be performed which ensures the proper contact of DUT tIo the pogo pins of the HIB. Test is performed considering the ESD diode of each pin of an IC. The structure of the ESD Diode is shown in Fig. 3, and the results for continuity test are shown in Fig. 4. A result shows the measured voltage for each pin of the device.

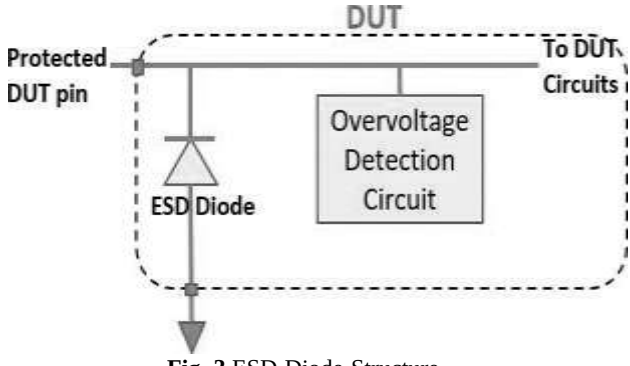

Fig. 3.ESD Diode Structure

Datalog for Serial#: 6, Site #3, Bin #01
Wafer Coordinates: (6, 0)

TEST#	RESULT	UNITS	LOWER	UPPER	ALARM	TEST NAME
1.1	-0.645	V	-1.000	-0.300		Conty_Pin1
1.2	-0.617	V	-1.000	-0.300		Conty_Pin2
1.3	-0.629	V	-1.000	-0.300		Conty_Pin3
1.4	1.986	V	1.500	2.500		Conty_Pin4
1.5	1.923	V	1.500	2.500		Conty_Pin5
1.6	1.251	V	1.000	2.000		Conty_Pin6
1.7	-0.855	V	-1.000	-0.300		Conty_Pin7
1.8	0.480	V	0.300	1.800		Conty_Pin8
1.9	-0.630	V	-1.000	-0.300		Conty_Pin9
1.10	-0.630	V	-1.000	-0.300		Conty_Pin10
1.11	-0.630	V	-1.000	-0.300		Conty_Pin11
1.12	-0.492	V	-1.000	-0.300		Conty_Pin12
1.13	-0.483	V	-1.000	-0.300		Conty_Pin13
1.14	-0.483	V	-1.000	-0.300		Conty_Pin14

Fig. 4. Continuity Test Results

Low Voltage Leakage (LVL): Test to ensure no leakage current when device is not enabled. The result for the test is shown in Fig. 5.

Datalog for Serial#: 20, Site #3, Bin #09
Wafer Coordinates: (16, 0)

TEST#	RESULT	UNITS	LOWER	UPPER	ALARM	TEST NAME
7.1	0.065	nA	-499.000	499.000		PIN1_POS
7.2	0.666	nA	-999.000	999.000		PIN2_POS
7.3	0.290	nA	-99.000	99.000		PIN3_POS
7.4	10.858	nA	-999.000	999.000		PIN4_POS
7.5	197.271	nA	-999.000	999.000		PIN5_POS
7.6	208.445	nA	-999.000	999.000		PIN6_POS
7.7	-0.433	nA	-499.000	499.000		PIN7_POS
7.8	-4.510	nA	-499.000	499.000		PIN1_NEG
7.9	-9.521	nA	-999.000	999.000		PIN2_NEG
7.10	0.075	nA	-99.000	99.000		PIN3_NEG
7.11	-229.988	nA	-999.000	999.000		PIN4_NEG
7.12	-201.703	nA	-999.000	999.000		PIN5_NEG
7.13	-203.167	nA	-999.000	999.000		PIN6_NEG
7.14	-1.165	nA	-499.000	499.000		PIN7_NEG
7.15	205.338	nA	-999.000	999.000		PIN8_POS
7.16	0.769	nA	-999.000	999.000		PIN9_POS
7.17	1666.657	nA	-999.000	999.000	FAIL	PIN10_POS
7.18	-206.388	nA	-999.000	999.000		PIN8_NEG
7.19	-0.173	nA	-999.000	999.000		PIN9_NEG
7.20	-12133.610	nA	-999.000	999.000	FAIL	PIN10_NEG

Fig. 5. Low Voltage Leakage Test Results

Quality Analysis Tests

Turn On time (t_{ON}): t_{ON} is the total time from 50% EN rising to the 90% of V_{out} rising. From Fig. 6 t_{ON} for this high side switch is 70uS.

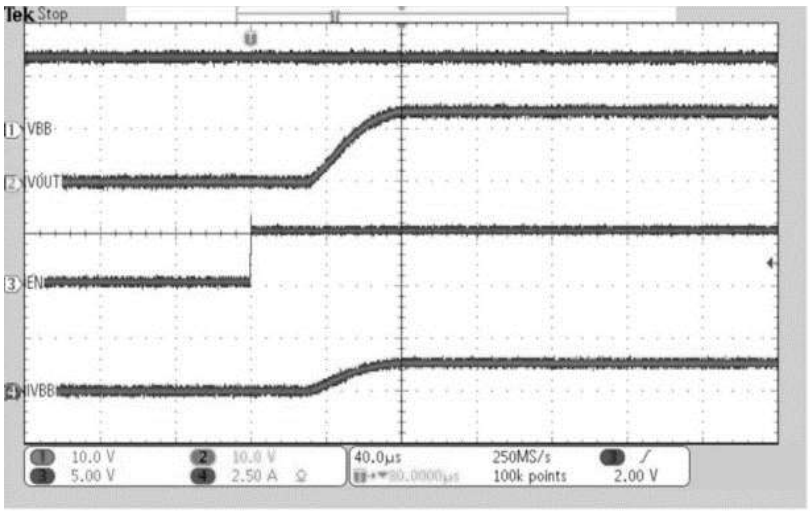

Fig. 6. Turn On time (t_{ON})

- **Turn Off time(t_{OFF}):** t_{OFF} is the total time from 50% EN falling to the 10% of V_{out} falling. From Fig.7 t_{OFF} for this high side switch is 65uS.

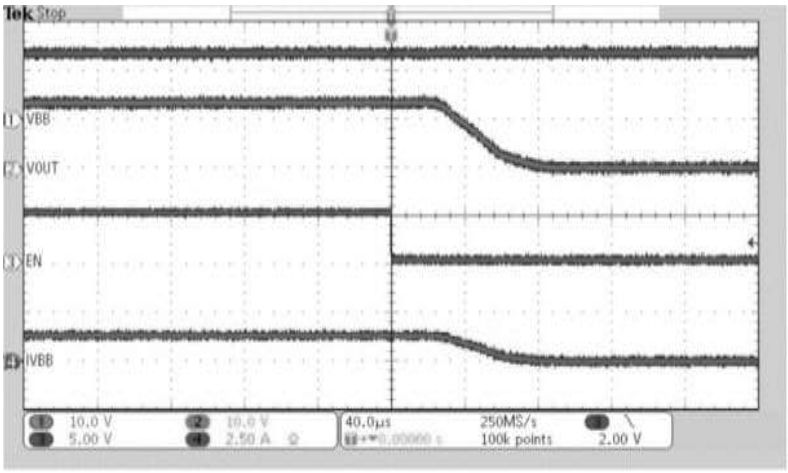

Fig. 7. Turn Off time (t_{OFF})

- **V_{SNS} for I_{VBB}:** I_{SNS} is the sensed current of I_{VBB} with scale down (I_{SNS}=I_{OUT}/Ksns).Ksns for the deviceis 1250. I_{OUT} is being swept from 500mA to 3A, butbecause of the current limit feature I_{VBB} is regulated to2.5A. The sensed current I_{SNS} follows I_{VBB} shown in Fig. 8. As, I_{SNS} = (2.5A/1250) = 2mA, V_{SNS} = (2mA/1KOhm) = 2V.

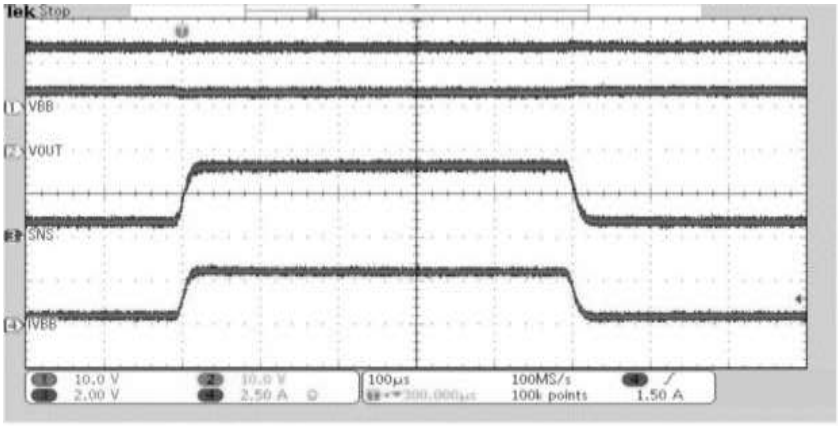

Fig. 8. V_{SNS} for I_{VBB}

- **5mH Inductive Load Driving:** When an inductiveload is switching off, the output voltage is pulled down to negative, due to the inductance characteristics. The power FET can break down if the voltage is not clamped during the current-decay period. To protect the power FET in this situation, internally clamp the drain-to-source voltage, namely V_{DS} clamp.

  Fig. 9 and 10 shows that, when load is switched off, the V_{OUT} is clamped to 0V in order to protect the FETand observe that I_{VBB} is falling down to 0 ampere because EN is made low.

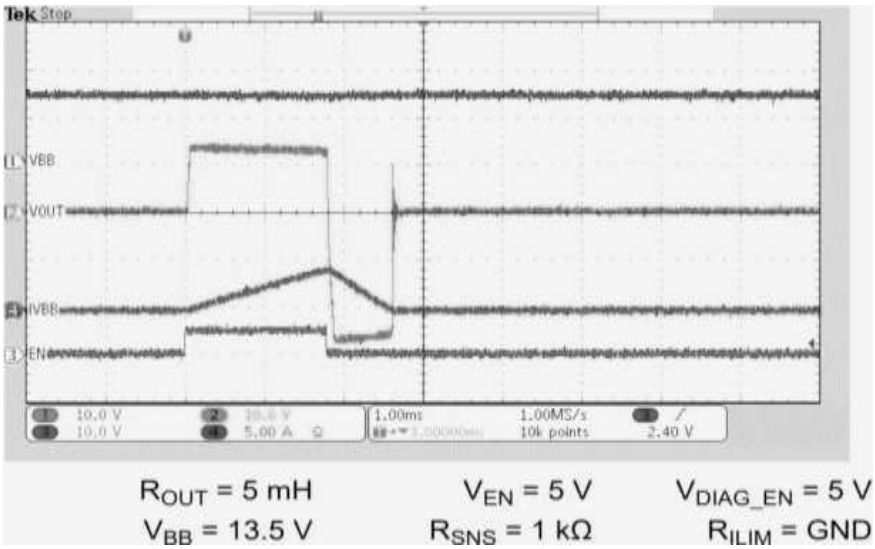

Fig. 9. 5mH Inductive Load Driving

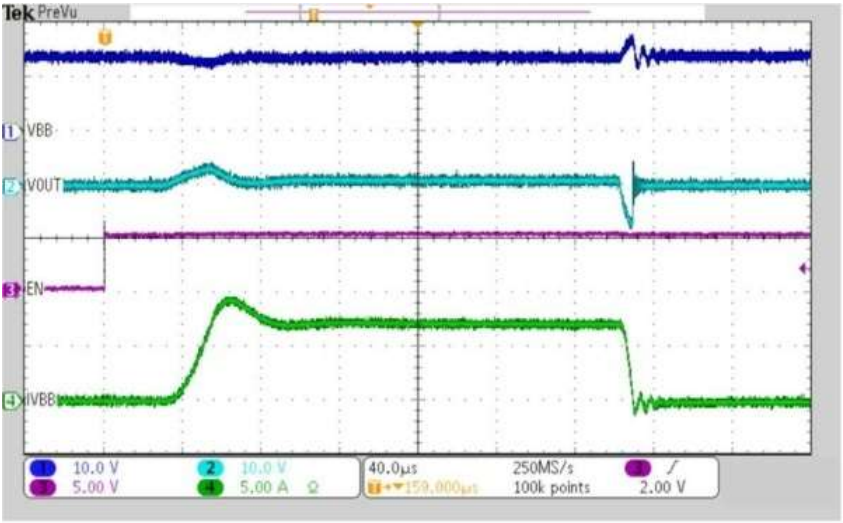

Fig. 10. I_{VBB} With RILIM Shorted to Ground

4.0 Results and Discussions

Characterization: Over the IC's working temperature range, various parameters are examined and based on the results, the analysis has been made to observe how well the IC works at different temperatures [14].

- Standby Current is the current drawn by the IC in its OFF state. Based on the characterization of standby current (I_{sb}) the plot is obtained. From Fig. 11, the standby current I_{sb} remains constant till some point of temperature and then starts increasing as semiconductors have negative temperature coefficient.
- Quiescent Current is the current drawn by the IC in its ONstate. Based on the characterization of Quiescent current (IQ) the plot is obtained. The IQ is constant over the temperature but varies with the variation of voltage shown in Fig. 12.

Diagnostic Current is the current drawn by the IC when DIAGEN = High and EN = Low. Since in this condition, the diagnostics are available the IC draws some amount of current. Based on the characterization of Dianostic current (IDIAG) the plot is obtained and shown in Fig. 13. Here IDIAG is constant over the temperature but varies with the variation of voltage.

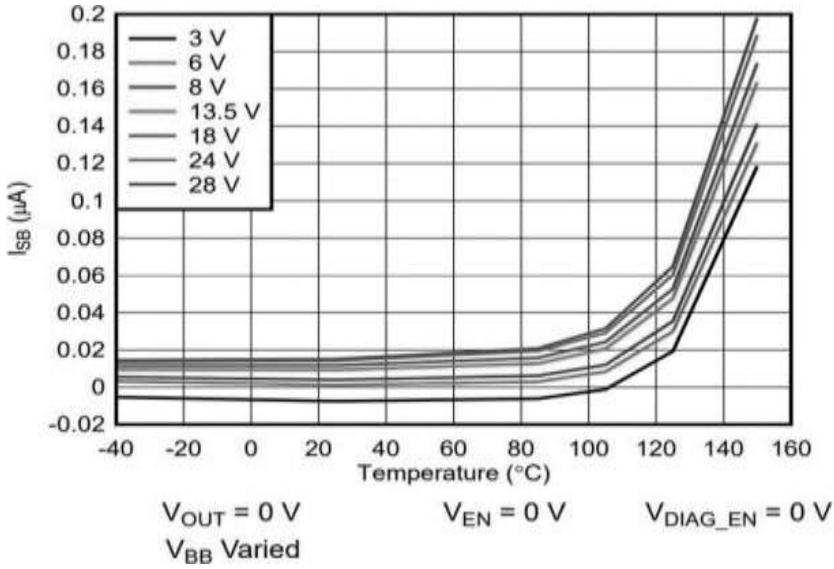

Fig. 11. Standby Current I_{sb} vs Temperature

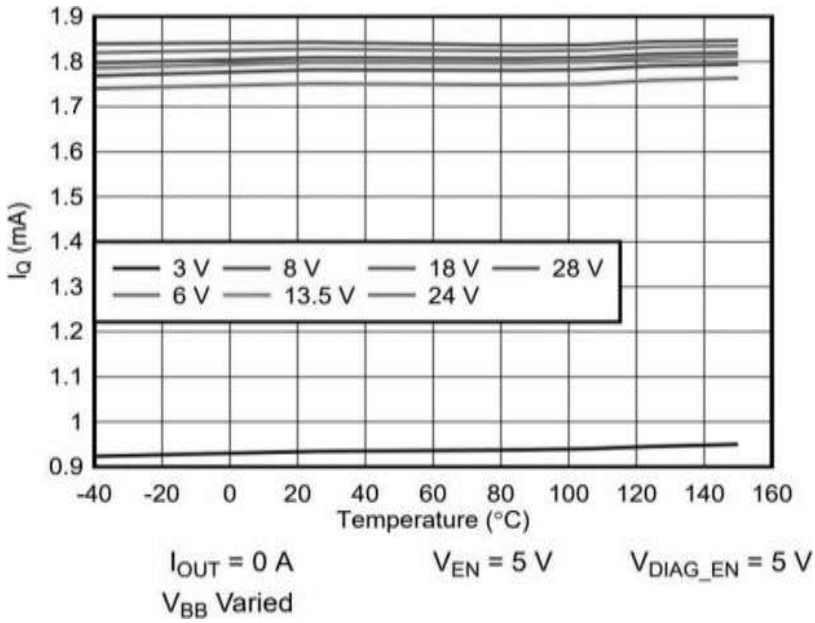

Fig. 12. Quiescent Current IQ vs Temperature

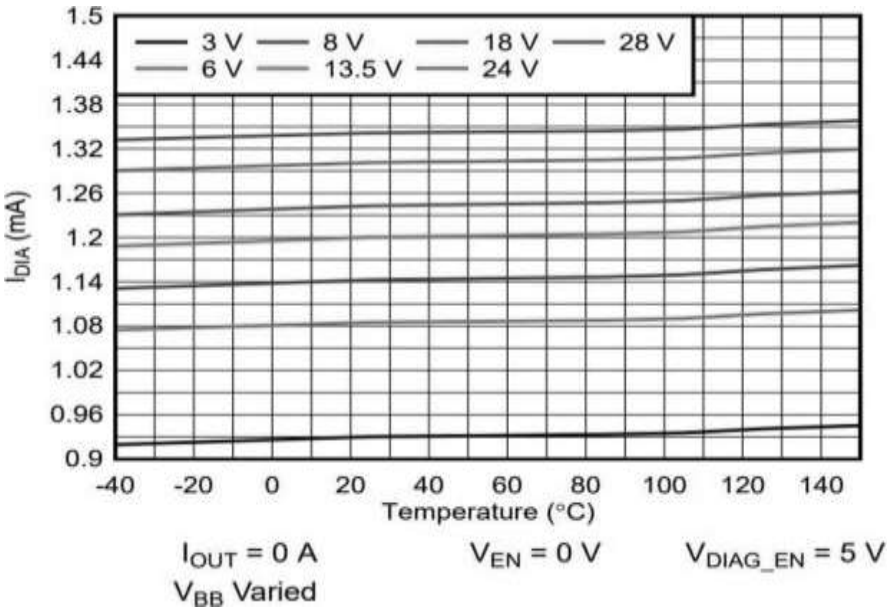

Fig. 13. Diagnostic Current IDIAG vs Temperature

5.0 Conclusion

The plan for a Final Test solution of a Smart High Side Switch is presented in this paper. The need for High Side Switch is appreciated starting with a basic understanding of High Side Switches. After properly understanding the IC's performance, a test plan, which is report providing information on the tests to be performed, the testing scope of these parameters, and pin details, is developed. The Test Plan was formed for the purpose of reducing tester errors as much as possible. A feasibility study is conducted to ensure that the Eagle test platform can be used for the High Side Switch's final test solution. The basic test program was developed in Eagle Software and tested on the device using ETS Tester. Characterization is performed on the High Side Switch to better analyze the quality of the IC over different temperature conditions and the critical tests among them are noted in the results.

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